CERTIFICATION OF TRANSLATION

I, Yeonsook Yun, an employee of Y.P.LEE, MOCK & PARTNERS of The Cheonghwa Bldg., 1571-18 Seocho-dong, Seocho-gu, Seoul, Republic of Korea, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statements in the English language in the attached translation of the priority document (Korean Patent Application No. 00-70008), consisting of 15 pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 8 day of October, 2004

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SPECIFICATION

[Title of the Invention]

Solution for chemical mechanical polishing and method of manufacturing copper metal interconnection layer using the same

[Brief Description of the Drawings]

FIG. 1 is a sectional view for illustrating a copper seed layer including contaminant abrasives after CMP process using a conventional solution; and

FIGS. 2 through 5 are sectional views for illustrating processes in manufacturing a copper metal interconnection layer using a chemical mechanical polishing (CMP) solution according to an embodiment of the present invention.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a chemical mechanical polishing (CMP) solution, and more particularly to a CMP solution to polish a copper metal interconnection layer.

As semiconductor devices become highly efficient and highly integrated, multi-layered interconnection layers are used in the design and manufacturing processes. In a multi-layered interconnection layer, after one process is completed, for example the formation of an insulator, deposition of a metal interconnection layer, or the like, a CMP process is performed for planarizing a base layer to more easily perform subsequent processes such as photolithography.

To enhance polishing operation efficiency, a solution for the CMP process may be used. Generally, the CMP process is performed using both mechanical operation of a polisher and chemical reactions of a solution composed of chemical solutions and polishing particles. When a wafer surface contacts a pad, a solution for CMP process flows into a minute gap between the contact surfaces of the wafer and the pad, so that a

mechanical operation is performed by abrasive particles within the solution and bumps on the surface of the pad, and a chemical removing operation is performed by a chemical component within the solution.

In forming a semiconductor interconnection layer, it is important to reduce a (RC) value of a semiconductor device by having low resistance and low parasitic capacitance. In this case, the RC value is the product of the resistance and capacitance. Copper (Cu) has a lower resistivity than aluminum (Al). Therefore, with a semiconductor design rule of 0.18 μm, a metal interconnection layer process is high in demand to reduce interconnection resistance and parasitic capacitance. A metal interconnection layer using aluminum is formed by a photolithography process: i.e., first, a metal interconnection material is coated on the substrate and then the metal interconnection material is patterned. However, a metal interconnection layer using copper is usually formed differently because of difficulties in the patterning process. That is, a metal interconnection region is formed within an interdielectric layer on the substrate, then the metal interconnection material is buried in the metal interconnection region. For this purpose, in general, a damascene process is used. Metal interconnection structures formed using the damascene process are divided into a line damascene structure and a dual damascene structure. In the line damascene structure, a trench having a predetermined depth from a surface of an interdielectric layer is formed in a line form, and an interconnection metal layer is formed within the trench. In the dual damascene structure, a contact hole or a via hole is buried to connect a metal interconnection layer buried in a line form within a trench region to a lower conductive layer.

According to a conventional method of forming a copper interconnection layer, a line-like trench region is formed in an interdielectric layer. Then, a barrier layer is formed along a stepped portion over the entire surface of the interdielectric layer, and then a copper seed layer is formed using physical vapor deposition. A copper layer is formed on the result by electroplating to completely cover the trench, and then CMP is performed to form a copper metal interconnection layer. However, the method of manufacturing the metal interconnection layer including CMP has many disadvantages.

First, through-put decreases and production costs increase since the amount of the copper interconnection layer to be removed is large. Second, since the amount of copper interconnection layer to be removed is large, uniformity deteriorates during CMP. Ultimately, a metal interconnection layer formed in a substrate has varying thinknesses. Third, when a copper layer is removed using CMP, the dielectric layer erodes due to density difference of the metal interconnection layer. As a result, the metal interconnection layer formed in a substrate has varying thickness, thus resulting in defects of products. Fourth, when the seed layer and the barrier film are polished at different polishing speeds, different solutions must be used. That is, the need of different solutions makes CMP complex and expensive.

In order to solve these problems, a method has been introduced after the copper seed layer is formed. In detail, while a copper seed layer formed inside a trench, in which an interconnection layer is to be formed using CMP, is left, an upper copper seed layer is removed by polishing. Then, only the copper seed layer formed inside the trench is electroplated to form a copper interconnection layer. However, in this case, when a conventional solution containing alumina or silica is used during CMP, abrasives (polishing particles) remain within the trench that is an interconnection region. The removal of such abrasives is very difficult. Further, such a problem become worse when semiconductor devices are highly integrated. In particular, a dual damascene process, in which an interconnection layer and a contact plug are formed at the same time, is much susceptible to this problem compared a line damascene process in which only an interconnection line is formed. In addition, the abrasives cause wafer contamination, wafer scratch, more seriously, lifting phenomenon of the metal interconnection layer, or the like.

FIG. 1 is a sectional view illustrating a copper seed layer having abrasives as a contaminant after CMP process using a conventional solution. Referring to FIG. 1, a reference numeral 10 denotes an interdielectric layer, a reference numeral 12 denotes a trench, a reference numeral 14 is a barrier layer, and a reference number 16 denotes a copper seed layer.

[Technical Goal of the Invention]

The present invention provides a solution for chemical mechanical polishing (CMP) to prevent a wafer contamination, scratch on a wafer surface, or the like, which are caused by abrasives.

The present invention also provides a method of manufacturing a copper metal interconnection layer to prevent abrasives from remaining within a recessed (or trench) region.

[Structure of the invention]

According to an aspect of the invention, there is provided a CMP solution including an oxidizing agent, a pH controlling agent, a chelate reagent, and deionized water. Preferably, the CMP solution does not include an abrasive.

The solution may be used when a copper metal interconnection layer is polished using CMP.

The oxidizing agent is preferably a hydrogen peroxide, an oxidizing agent of a ferric series or an oxidizing agent of an ammonium series.

A pH of the solution may be in the range of about 2 to about 11.

A pH controlling agent may be an acidic or a basic solution.

The chelate reagent may be citric acid, malic acid, gluconic acid, gallic acid, tannic acid, ethylenediaminetetraacetic acid (EDTA), benzotriazole (BTA), NHEDTA, nitrilotriacetic acid (NTA), DPTA or EDG.

According to another aspect of the invention, there is provided a method of manufacturing a copper metal interconnection layer including: forming a recessed region having a predetermined interconnection form in an interdielectric layer; forming a barrier layer along a stepped portion over the entire surface of the interdielectric layer having the recessed region; forming a copper seed layer on the barrier layer; and exposing the barrier layer by CMP using the abrasive-free solution according to the present invention until a surface of the interdielectric layer is exposed so that the copper

seed layer remains only within the recessed region.

The method of manufacturing a copper metal interconnection layer may further includes forming a copper layer on the copper seed layer formed in the recessed region; and forming a copper metal interconnection layer by planarizing the copper layer projecting above the surface of the interdielectric layer, and the barrier layer projecting above the surface of the interdielectric layer.

The present invention now will be described more fully hereinafter with reference to the preferred embodiments of the invention, and drawings for illustrating the embodiments. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the concept of the invention to those skilled in the art. The same reference numerals in different drawings represent the same elements.

According to a preferred embodiment of the present invention, a solution for CMP relates to a solution used for manufacturing a copper (Cu) metal interconnection, and more particularly, to a solution for CMP without an abrasive. That is, a conventional solution essentially includes an abrasive such as alumina (Al_2O_3) or silica (SiO_2), and the abrasive may remain within a wafer after CMP process, and the remaining abrasive may scratch the surface of the wafer. However, the solution according to a preferred embodiment of the present invention does not include the abrasive, thus avoiding the above problems caused by abrasive.

The solution for CMP according to a preferred embodiment of the present invention includes an oxidizing agent, a pH controlling agent, a chelate reagent, and deionized water.

The oxidizing agent is, preferably, hydrogen peroxide (H_2O_2), an oxidizing agent of a ferric series, or an oxidizing agent of an ammonium series. If hydrogen peroxide (H_2O_2) is used as the oxidizing agent, the hydrogen peroxide preferably has a concentration of about 1% to about 20% by weight, and more preferably, about 1% to about 10% by weight. If an oxidizing agent of the ferric series such as $Fe(NO_3)_3$ or

$Fe(PO_4)_3$ is used, the oxidizing agent of the ferric series preferably has a concentration of about 0.01% to about 5% by weight, and more preferably, about 0.01% to about 1% by weight. If an oxidizing agent of the ammonium series such as NH_4NO_3 or $NH_4(PO_4)$ is used, the oxidizing agent of the ammonium series preferably has a concentration of about 0.01% to about 5% by weight, and more preferably, about 0.01% to about 1% by weight.

According to a preferred embodiment of the present invention, the pH of the solution for CMP is preferably between about 2 and about 11. The pH of the solution is controlled with an acidic solution or a basic solution. As an acidic pH controlling agent, an acid solution such as sulfuric acid (H_2SO_4) solution, nitric acid (HNO_3) solution, hydrochloric acid (HCl) solution or phosphoric acid (H_3PO_4) solution may be used. As a basic pH controlling agent, a basic solution such as potassium hydroxide (KOH) solution or ammonium hydroxide (NH_4OH) solution may be used.

As the chelate reagent, citric acid, malic acid, gluconic acid, gallic acid, tannic acid, ethylenediaminetetraacetic acid (EDTA), benzotriazole (BTA), NHEDTA, nitrilotriacetic acid (NTA), DPTA or EDG may be used. The chelate reagent preferably has a concentration of about 0.001% to about 1% by weight, and more preferably, about 0.001% to about 0.1% by weight.

According to a preferred embodiment of the present invention, copper removal rate by the CMP is about 1000 Å/min through about 2000 Å/min, tantalum (Ta) removal rate by the CMP is about 200 Å/min through about 500 Å/min, tantalum nitride (TaN) removal rate by the CMP is about 200 Å/min through about 500 Å/min, and plasma enhanced tetraethyl ortho-silicate (PE-TEOS) is removed at a rate lower than about 50 Å/min.

Hereinafter, a manufacturing method of a metal interconnection using a solution for CMP process according to a preferred embodiment of the present invention will be described.

FIGS. 2 through 5 are sectional views illustrating processes in a method of manufacturing a copper metal interconnection using a solution for CMP process of the

present invention.

Referring to FIG. 2, recessed regions 22 are formed on an interdielectric layer 20 which is formed on a semiconductor substrate (not shown) using a photolithography and an etching process. In a line damascene structure, the recessed regions 22 may be trenches having a predetermined depth within the interdielectric layer 20. However, In a dual damascene structure, the recessed region 22 may be contact holes or via holes which penetrate the interdielectric layer 20 and expose a lower layer, such as the semiconductor substrate (not shown) or the lower interconnection layer (not shown), or the recessed regions 22 may be a combination of trenches, contact holes and via holes.

Then, a barrier layer 24 is formed along a stepped portion on the surface of the interdielectric layer 20 having the trenches. The barrier layer 24 is preferably formed of a material such as titanum (Ti), titanum nitride (TiN), tantalum (Ta) and tantalum nitride (TaN) which can prevent diffusion of a metal, and act as an adhesive layer between the interdielectric layer 20 and a metal interconnection to be formed.

Next, a copper (Cu) seed layer 26 is formed along a stepped portion on the barrier layer 24 by depositing copper using a physical vapor deposition (PVD) method such as sputtering.

Referring to FIG. 3, CMP is performed using the solution of the present invention to polish and remove the upper copper seed layer 26, and then, a trench copper seed layers 26a are formed in the recessed regions 22 where a metal interconnection is to be formed, and the surface of the barrier layer 24 except in the recessed regions 22 is exposed. A conventional solution including abrasives may leave abrasives in the trenches 22 where the interconnection will be formed after the CMP process, and causes problems such as contamination of a wafer, and more seriously, lifting of the interconnection. Also, the abrasive scratches the wafer. However, if the CMP process is performed using a solution without an abrasive according to the present invention, the problems of the conventional solution, such as scratching of the wafer caused by abrasive and abrasive remaining within the trenches, do not exist.

Referring to FIG. 4, copper layers 28 are formed on the trench copper seed

layers 26a by a normal electroplating process to fill the recessed region 22. Here, since the electroplating process is done only in the region where the trench copper seed layers 26a are formed, the copper layers 28 are formed within the recessed regions 22. In this case, the copper layers 28 may be thick enough to cover the recessed regions 22.

Referring to FIG. 5, portions of the copper layer 28 projecting above the surface of the interdielectric layer 20, and portions of the barrier layer 24 projecting above the surface of the interdielectric layer 20 are removed by second CMP process to form a copper metal interconnection layer 28a filling the recessed regions 22.

While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.

[Effect of the Invention]

The use of a solution for CMP and a manufacturing process of a copper metal interconnection layer using the solution according to the present invention may include many advantages.

First, since an abrasive in the CMP solution is not included, various defects such as contamination of the wafer by remaining abrasives or scratching by abrasives are removed or substantially entirely eliminated.

Second, since an abrasive is not included in the solution, the manufacturing costs for the solution is low and CMP process is less expensive.

Third, since the copper layer is formed only within the recessed region where the interconnection is to be formed, it is not necessary for the copper layer to be thick. Thus, the required amount of CMP for forming the copper metal interconnection is largely reduced.

Fourth, since only a small amount of the copper layer is polished, uniformity of

the surface of the wafer having copper metal interconnection layer is excellent. Also, since excess CMP is not required, dishing or erosion of an interdielectric layer can be prevented.